## CLAIMS

What is claimed is:

1. A hybrid serial/parallel bus interface for a base station comprising:

a data block demultiplexing device having an input configured to receive a data block and demultiplexing the data block into a plurality of nibbles, each nibble having a plurality of bits;

for each nibble:

a parallel to serial converter for converting that nibble into serial data;

a line for transferring that nibble serial data; and

a serial to parallel converter for converting that nibble serial data to recover that nibble; and

a data block reconstruction device for combining the recovered nibbles into the data block.

2. The base station interface of claim 1 wherein a number of bits in a data block is N and a number of the lines is i and $1 < i < N$.

3. The base station interface of claim 1 wherein a number of bits in a nibble is four and a number of lines is two.

4. A hybrid serial/parallel bus interface for a base station comprising:

means having an input configured to receive a data block for demultiplexing the data block into a plurality of nibbles, each nibble having a plurality of bits;

for each nibble:

means for converting that nibble into serial data;

a line for transferring that nibble serial data; and

means for converting that nibble serial data to recover that nibble; and

means for combining the recovered nibbles into the data block.

5. The base station interface of claim 4 wherein a number of bits in a data block is N and a number of the lines is i and $1 < i < N$.

6. The base station interface of claim 4 wherein a number of bits in a nibble is four and a number of lines is two.

7. A base station having hybrid serial/parallel bus interface for transferring data from a first node to a second node, the interface comprising:

a data block demultiplexing device for demultiplexing a data block from the first node into m sets of n bits and for adding a start bit to each of the m sets, the m start bits collectively representing one of a particular function to be performed or a destination;

for each of the m sets, a separate line for transferring that set of the m sets from the first node to the second node;

a data block reconstruction device for receiving the m sets, for combining the m sets into the data block and for utilizing the m sets in accordance with the m start bits.

8. The base station interface of claim 7 wherein the demultiplexing device sets at least one of the m start bits in a one state when transmitting data and when the interface is not transmitting data, maintains all the separate lines in a zero state.

9. The base station interface of claim 7 wherein the m start bits represent a start of data transfer.

10. The base station interface of claim 7 wherein the m start bits collectively represent a particular function to be performed and not a destination.

11. The base station interface of claim 7 wherein functions that the m start bits collectively represent include a relative increase, a relative decrease and an absolute value function.

12. The base station interface of claim 7 wherein the m start bits collectively represent a particular destination and not a function to be performed.

13. The base station interface of claim 12 wherein destinations that the m start bits collectively represent include an RX and TX gain controller.

14. The base station interface of claim 7 wherein the m start bits collectively represent both a particular function to be performed and a particular destination.

15. A base station having a hybrid serial/parallel bus interface for transferring data from a first node to a second node, the interface comprising:

means for demultiplexing a data block into m sets of n bits;

means for adding a start bit to each of the m sets, the m start bits collectively representing one of a particular function to be performed or destination;

means for transferring from the first node each of the m sets over a separate line;

means for receiving at the second node each of the transferred m sets; and

means for utilizing the received m sets in accordance with the m start bits.

16. The base station interface of claim 15 wherein the adding means sets at least one of the m start bits to a one state and when the interface is not transmitting data, all the separate lines to a zero state.

17. The base station interface of claim 15 wherein at least one of the m start bits represents a start of data transfer.

18. The base station interface of claim 15 wherein the m start bits collectively represent a particular function to be performed and not a destination.

19. The base station interface of claim 15 wherein functions that the m start bits collectively represent include a relative increase, a relative decrease and an absolute value function.

20. The base station interface of claim 15 wherein the m start bits collectively represent a particular destination and not a function to be performed.

21. The base station interface of claim 20 wherein destinations that the m start bits collectively represent include an RX and TX gain controller.

22. The base station interface of claim 15 wherein the m start bits collectively represent both a particular function to be performed and a particular destination.

23. A base station hybrid serial/parallel bus interface for use in a synchronous system, the synchronous system having an associated clock, the bus interface, comprising:

a data block demultiplexing device having an input for receiving a data block and demultiplexing the data block into a plurality of nibbles, each nibble having a plurality of bits;

an even and an odd set of parallel to serial (P/S) converters, each set of P/S converters receiving the nibbles synchronous with a clock rate of the clock, and for converting the nibbles into a serial data;

a first set of i multiplexers for serially transferring data from the set of even P/S converters on a positive edge of the clock over i lines and serially transferring data from the set of the odd P/S converters on a negative edge of the clock over i lines;

a second set of i demultiplexers for receiving the even and odd serial data and sending the even received serial data to an even buffer and the odd serial data to an odd buffer;

an even and an odd set of serial to parallel (S/P) converters, the even set of S/P converters converting the received even serial data to even parallel data and outputting the even parallel data synchronous with the clock;

the odd set of S/P converters for converting the odd received serial data to odd parallel data and outputting the odd parallel data synchronous with the clock; and

a data block reconstruction device for combining the even and odd parallel data as the data block.

24. The base station interface of claim 23 wherein each data block has N bits and $1 < i < \frac{N}{2}$.

25. The base station interface of claim 23 wherein the even and the odd buffers respectively buffer the outputs of the even and odd set of P/S converters so that the even and odd set of S/P converters receive the even and odd received serial data synchronous with the clock.

26. A bi-directional serial/parallel bus interface employed by a base station comprising:

a plurality of lines for transferring data blocks, the plurality of lines being less than a number of bits in each data block;

a first node sending first data blocks to a second node over the plurality of lines, the first node demultiplexing the data block into a plurality of first nibbles, the plurality of first nibbles being equal in number to the plurality of lines, each first nibble having a plurality of bits; and

the second node sending second data blocks to the first node over the plurality of lines, the second node demultiplexing the data block into a plurality of second nibbles, the plurality of second nibbles being equal in number to the plurality of lines, each second nibble having a plurality of bits.

27. The base station interface of claim 26 wherein the first node demultiplex the data block into a plurality of third nibbles, a number j of the third nibbles is less than the number N of lines and transferring the third nibbles over j lines.

28. The base station interface of claim 27 wherein the second node demultiplexes fourth data blocks into K bits, where K is less than or equal to N-j lines, and transferring the fourth data block over K lines.

29. The base station interface of claim 26 wherein the first node data blocks include gain control information.

30. The base station of claim 29 wherein the second node data blocks include an acknowledgment of receipt of the gain control information.

31. The base station interface of claim 29 wherein the second node data blocks include information of a status associated with the second node.

32. A gain control (GC) employed by a base station, comprising:

a GC controller for producing a data block having n bits representing a gain value;

i lines for transferring the data block from the GC controller to a GC, where $1<i<n$; and

the GC for receiving the data block and adjusting a gain of the GC using the gain value of the data block.

33. The base station GC of claim 32 further comprising:

a data block demultiplexing device for demultiplexing the data block into a plurality of nibbles, each nibble being transferred over a different line of the i lines; and

a data block reconstruction device for combining the nibbles into the data block.

34. The base station GC of claim 33 wherein appended to each nibble is a start bit.

35. The base station GC of claim 34 wherein the start bits indicate a function to be performed.

36. The base station GC of claim 35 wherein mathematical functions indicated by the start bits include a relative increase, a relative decrease and an absolute value function.

37. The base station GC of claim 34 wherein the GC includes a RX GC and a TX GC and the start bits indicate whether the data block is sent to the RX GC or TX GC.